

REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1, 3-6, 11-15, 17 and 19-26 are now present in this application. Claims 9 and 10 are canceled as being redundant, as pointed out by the Examiner. Claims 1, 15 and 22 are independent. Claim 1 is amended. No new matter is involved.

Reconsideration of this application, as amended, is respectfully requested.

Objections to Claims

Claims 1 and 15 are objected to for various informalities. These objections are respectfully traversed.

Claim 1 has been amended to obviate the objection, as follows: --a low reflective layer for covering at least a portion of at least one of said gate line and said data line and on covering the area to shield the light passing the gate line, the data line and the area;--

Support for this is found throughout the Application as originally filed including, for example, in the last paragraph on page 7, and in Figs, 5 and 6.

This Amendment does not narrow the scope of claim 1 in any manner, it merely clarifies its meaning.

Claim 15 is objected to for reciting "forming an insulating layer electrically insulating said gate line and the gate electrode." The Office Action states that this claim should recite an insulating layer electrically insulating the gate line and the gate electrode from the data line.

Applicants respectfully disagree.

The Office Action explains why the gate electrode is not insulated from the gate line. Applicant agrees with the analysis. However, the language in issue, which is also found in claim 22 and is not objected to in claim 22, does not state forming an insulating layer electrically insulating the gate line from the gate electrode. The language in issue merely recites forming an insulating layer separating both the gate electrode and the gate line. It does not state what those elements are insulated from, nor does it have to.

As pointed out in the Amendment filed on March 14, 2005, this language is found in originally filed claim 22, so there is proper basis for the language as part of Applicant's originally filed disclosure, and no previous Office Action has found a problem with this language. Nor does this Office Action find fault with the identical language in claim 22.

Applicants also respectfully submit that they are entitled to claim what they regard as their invention, especially, as here, where open-ended claim terminology is used.

Reconsideration and withdrawal of these objections are respectfully requested.

Furthermore, the arguments set forth above were set forth in the Amendment filed on March 14, 2005 but have not been addressed by the Examiner as required by MPEP §707.07(f). This failure to address all of Applicants' arguments denies Applicants fundamental substantive and procedural due process under the Administrative Procedures Act, which governs USPTO patent examination procedures. See in this regard, In re Zurko, 119 S.Ct. 1816, 50 USPQ2d 1930 (1999), and In re Gartside, 53 USPQ2d 1769 (Fed. Cir. 2000).

Rejections under 35 U.S.C. §103

Claims 1, 11, 14-15, 22 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,259,200 to Morita et al. (hereinafter, "Morita"). This rejection is respectfully traversed.

Complete discussions of the rejections are set forth in the Office Action and are not being repeated here.

Independent claims 1, 15 and 22 recite a combination of features regarding a liquid crystal display (LCD) including (1) a pixel electrode having portions thereof formed on the surface of the passivation layer but not over the thin film transistor; and an upper substrate located above the pixel electrode, wherein an

area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black matrix or light shielding layer, or (2) a method of making the structure set forth in (1).

Applicants respectfully submit that this combination of elements as set forth in independent claims 1, 15 and 22 is not disclosed or made obvious by the prior art of record.

Morita only discloses a low reflective layer 10x on its source line 10 "to preclude unwanted light reflection" (col. 4, lines 51-67). Morita does not disclose a low reflective metal layer disposed on one of the gate line and data line and the area having a channel area, a source area and a drain area, as recited. Moreover, Morita's upper substrate above the pixel electrode does disclose a black mask 62, which is a black layer and/or a light shielding layer. This is just the opposite of what is recited in all of the claims.

Thus, Morita does not disclose or suggest the claimed invention.

The Office Action concludes that it would be obvious to arrange the low reflective layer 10x on the data line or the gate line and on the channel area, source area, drain area, and to do away with the black matrix (actually, just a black layer 62) "for precluding light reflection."

Applicants respectfully disagree.

The Examiner has the initial duty of supplying the factual basis for the rejection he advances. An Examiner may not, because of doubts that the

invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis. See, In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968).

Moreover, in making a rejection under 35 U.S.C. §103, the prior art as a whole must be considered. The teachings of the applied references are to be viewed as they would have been viewed by one of ordinary skill in the art. Kimberly-Clark v. Johnson & Johnson, 745 F.2d 1437, 1454, 223 USPQ 603, 614 (Fed. Cir. 1984); In re Mercier, 515 F.2d 1161, 1165, 185 USPQ 774, 778 (CCPA 1975). "It is impermissible within the framework of §103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In re Wesslau, 353 F.2d at 241, 147, USPQ at 393. In re Hedges, et al., 228 USPQ 685 (Fed. Cir. 1986).

If it were so obvious to modify Morita to remove any black layer from the upper substrate and to provide a low reflectivity layer on the gate electrode and drain electrode as well as on the data line, then why didn't Morita do it?

The Office Action fails to offer any explanation of why Morita did not make the claimed invention. Applicants respectfully submit that it would not be

obvious to modify Morita so drastically as suggested because it would not have been obvious to do so.

Applicants note that the aforementioned argument was presented in the Amendment filed on March 14, 2005 but has not been addressed in the outstanding Office Action in violation of MPEP §707.07(f).

One reason it would not be obvious to modify Morita as suggested is because Morita teaches that the invention is “preferably provided with at least a shading black mask aligned with the gate line” and that the Morita device “needs to shade the row gate lines” (col. 2, 34-44).

These are positive teachings in the very same reference that provide the top layer with its signal lines 10 with low reflectivity layers 10x. Applicants respectfully submit that such positive teachings teach away from removing the black shade layer for the gate lines.

Moreover, because there is no teaching at all in Morita of using low reflectivity layers on the transistor electrodes, per se, and because Morita is well aware that such layers are provided on signal lines, and because there is no disclosed problem with Morita’s transistor electrodes, or with its gate lines and drain lines, Applicants respectfully submit that one of ordinary skill in the art would have no incentive to go to the trouble and expense of providing such low reflectivity coatings on all these electrodes and lines.

Applicants note that the aforementioned arguments were presented in the Amendment filed on March 14, 2005, but have not been addressed in the outstanding Office Action.

Applicants respectfully submit that the only basis for modifying Morita as suggested is based solely on improper hindsight reconstruction of Applicants' invention based solely on Applicants' disclosure. Accordingly, the Office Action does not provide proper motivation to one of ordinary skill in the art to apply a low-reflective film to the recited gate and drain line and transistor electrode areas of Morita. Nor does the Office Action provide proper motivation for one of ordinary skill in the art to modify Morita by removing Morita's black shading layer that is explicitly taught as being needed, being an essential part of Morita's "improved" black mask, disclosed throughout the patent to improve over the shortcomings of prior art black masks.

Further to the arguments set forth above, Applicants make reference to the two full paragraphs in col. 6 of Morita which discusses the improved black mask of Morita's invention (see col. 1, lines 62-63 which discusses the need for an improved black mask). Morita's improved black mask 62 shields the gate line 43, auxiliary lines 44, thin film transistors 3, and auxiliary capacitances Cs, while Morita's light-shielding film (shielding back light) is used as a black mask to prevent light passing through between the signal lines 10 and the pixel electrodes

14 and covers the domains where the liquid crystal orientation is disturbed at the edge portions of the pixel electrode 14.

In other words, a black mask is an essential part of Morita's invention.

On the other hand, Morita only devotes two sentences to the low reflectance layer on signal lines 10. All that Morita states, in the main body of its specification is "According to the present invention, the top insulating substrate 60 is provided with no black mask aligned with the signal lines 10. The top layer of the signal lines 10 of Al will cause its reflectance to be large enough to degrade the quality of image. For this reason, a top layer of a material (Cr, for example) having a relatively low reflectance is further applied on the Al film to preclude unwanted light reflection."

Instead of taking these two sentences in context, the Office Action takes them out of context and speculates that it would be obvious to fundamentally change the "improved" black mask of Morita by eliminating it all-together and substituting a low reflectance layer on everything covered by Morita's black mask.

At best this amounts to nothing more than an open an invitation to try such a speculative modification that Morita clearly did not try or disclose trying. In other words, there is nothing on Morita that would motivate one of ordinary skill in the art to drastically redesign Morita to eliminate Morita's improved black mask and substitute a low reflectance coating without any disclosure that such a drastic modification will produce an improved device.

In Applicants' view, the only possible suggestion for combining the applied prior art in the manner proposed by the Examiner to meet the above-noted claim features stems from hindsight knowledge derived from the Applicants' own disclosure. The use of such hindsight knowledge to support an obviousness rejection under 35 U.S.C. §103 is, of course, impermissible. See, for example, W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir, 1983), cert. denied, 469 U.S. 851 (1984).

Because of these shortcomings of the rejection, the rejection fails to make out a *prima facie* case of proper motivation to modify Morita and, therefore, means that the Office Action fails to make out a *prima facie* case of obviousness of the claimed invention because a showing of a suggestion, teaching, or motivation to combine the prior art references is an "essential evidentiary component of an obviousness holding." C.R. Bard, Inc. v. M3 Sys. Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998).

Thus, reconsideration and withdrawal of this rejection of claims 1, 11, 14, 15, 22 and 25 are respectfully requested.

Claims 3, 4, 17, 19 and 26 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita, as applied above, and further in view of U.S. Patent 6,172,728 to Hiraishi and U.S. Patent 6,172,723 to Inoue et al. ("Inoue").

This rejection is respectfully traversed.

Initially, Applicants respectfully submit that Morita does not make out a *prima facie* case of unpatentability of the claimed invention recited in the claims from which claims 3, 4, 17, 19 and 26 depend, i.e., claim 11 or claim 22, and neither Hiraishi nor Inoue are applied to remedy the aforementioned deficiencies of Morita.

Accordingly, this rejection is improper and should be withdrawn.

Moreover, Hiraishi provides gaps or notches in the gate lines and/or source lines to reduce areas where they overlap with the pixel electrodes and to reduce the parasitic capacitance of the device (col. 5, lines 45-65).

Applicants respectfully submit that one of ordinary skill in the art would not be motivated to modify Morita to overlap the pixel electrode with a gate line or data line based on Hiraishi when Hiraishi teaches minimizing such overlap and because such overlap will increase the parasitic capacitance of the device, which Morita teaches away from doing - see col. 7, lines 28-54, for example.

Furthermore, Morita discloses a backlit LCD device (see Figs. 2 and 3, for example) that does not indicate that it needs its display quality increased, whereas Hiraishi discloses a reflective LCD device that needs to have its display quality enhanced by using a low reflective film on its gate lines and source lines. The Office Action has not demonstrated that one of ordinary skill in the art would look to a reflective LCD display to modify a backlit display, especially where there is no indication of a need to improve the characteristics of the backlit LCD device.

Applicants note that although this argument, which was presented in the March 14, 2005, Amendment, is not addressed, per se, in the outstanding Office Action, the Office Action states, in the "Response to Arguments" section dealing with the Morita reference, that "Morita discloses an active-matrix display that is not limited to use back light." Applicants respectfully disagree and note, in this regard, that the only disclosed embodiments of Morita operate using back light – see, for example, Figs. 1A, 2, 3 and 9A of Morita.

Moreover, the outstanding Office Action admits that Hiraishi does not disclose placing a low reflectance coating on source or drain electrodes. The Office Action merely states that it would be obvious to provide such a feature in Morita as "at least an obvious variation" because "forming a low reflectance layer on the gate electrode and on the source/drain electrode would be the same principle and would have the same function." Applicants respectfully disagree. The "same principle and same function" arguments may apply to the doctrine of equivalence for patent infringement analysis, but the issue involved here is proper motivation to modify primary reference that does not have this feature in view of a secondary reference that also does not have this feature, and this analysis simply does not fit.

Furthermore, one of ordinary skill in the art would have no incentive to modify Morita in view of Hiraishi, as suggested, because Morita's transistor electrodes are all shielded by the Morita's "improved" black mask and do not need

the features provides by the low reflectance material. Additionally, the Office Action fails to address the additional masking and etching steps that may be needed to provide such a suggested feature, steps that may well give a disincentive to provide such a feature.

The Office then turns to Inoue as evidence “that lights are mixed with light reflected from the reflection electrode and this mixed light lowers the image display quality.” Inoue allegedly solves such a problem by patterning a low-reflection conductive film on a high conductive reflection film – col. 11, lines 34-50. The Office Action continues by stating that gate electrodes, source electrodes and drain electrodes are electrical conductive films and would benefit from a low reflective film to enhance image quality.

Applicants respectfully disagree with this speculative reasoning for a number of reasons.

Firstly, none of the three applied references, including Inoue, disclose providing a low reflection film on any of the transistor electrodes, so there is no objective factual evidence that any of the three references provide any motivation to do so.

Secondly, the only objective factual evidentiary basis for an incentive to provide a low reflective layer on the gate electrode, source electrode and/or drain electrode is found in Applicants’ disclosure, which may not be properly used against Applicants.

Thirdly, as pointed out above, one of ordinary skill in the art would have no incentive to modify Morita in view of Hiraishi, as suggested, because Morita's transistor electrodes are all shielded by the Morita's "improved" black mask and do not need the features provided by the low reflectance material. Additionally, the Office Action fails to address the additional masking and etching steps that may be needed to provide such a suggested feature, steps that may well give a disincentive to provide such a feature.

Fourthly, Hiraishi's invention deals with reflective LCDs, not back-lit LCDs and the Office Action has not shown that a teaching applicable to a reflective LCD will provide proper motivation to modify a back-lit LCD absent comparative data to show that the same conditions will exist in both devices. However, instead of providing objective factual evidence of this type, the Office Action merely provides speculation, which is not a proper basis for a rejection based on 35 U.S.C. §103(a).

Accordingly, the claimed invention recited in claims 3, 4, 17, 19 and 26 is not obvious in view of the applied references.

Reconsideration and withdrawal of this rejection of claims 3, 4, 17, 19 and 26 is respectfully requested.

Claims 12, 13, 23 and 24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi. This rejection is respectfully traversed.

Initially, Applicants respectfully submit that Morita does not make out a *prima facie* case of unpatentability of the claimed invention recited in the claims from which claims 12, 13, 23 and 24 depend, i.e., claim 11 or claim 22, and Hiraishi is not applied to remedy the aforementioned deficiencies of Morita.

Accordingly, this rejection is improper and should be withdrawn.

Moreover, Morita, the base reference in the applied reference combination, does not disclose overlap of its pixel electrodes 14 with its gate lines 43 or with its data (signal) lines 10, and Hiraishi discloses reducing such overlap to reduce parasitic capacitance – see col. 5, lines 45-54. In view of this explicit teaching in Hiraishi, there would be no incentive to modify Morita to provide overlap between pixel electrodes and either (or both) data lines or gate lines. In fact, there would be an explicit disincentive to make the proposed modification of Morita. Thus, Hiraishi actually teaches away from being combined with Morita, as suggested.

A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. See W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1550-51, 220 USPQ 303, 311 (Fed. Cir. 1983) (the totality of

a reference's teachings must be considered), cert. denied, 469 U.S. 851 (1984); In re Spinnoble, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969) (references taken in combination teach away since they would produce a "seemingly inoperative device"); In re Caldwell, 319 F.2d 254, 256, 138 USPQ 243, 245 (CCPA 1963) (reference teaches away if it leaves the impression that the product would not have the property sought by the applicant). See, In re Gurley, 31 USPQ2d 1130 (Fed. Cir. 1994).

Accordingly, the Office Action fails to make out a *prima facie* case of proper motivation to modify Morita as suggested and therefore fails to make out a *prima facie* case of obviousness of the claimed invention.

Reconsideration and withdrawal of this rejection of claims 12, 13, 23 and 24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi is respectfully requested.

Claims 5, 6, 9, 10, 20 and 21 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi, and further in view of "Applicants' admitted prior art (AAPA)".

Initially, it is pointed out that this rejection is moot with respect to claims 9 and 10, which have been canceled as being respective duplicates of claims 5 and 6.

This rejection is respectfully traversed at least for the reasons that claim 1, from which claims 5, 6, 9 and 10 depend, and claim 15, from which claims 20 and

21 depend, are traversed, above. Additionally, Applicants have not made a clear, unequivocal and unmistakable admission of any prior art, including the “related art” disclosed in Figs. 1-4. The Office Action has not presented any objective factual evidence to support a conclusion that Applicants have made a clear, unmistakable and unequivocal admission that Figs. 1-4 are prior art to Applicants.

Moreover, the fact that CrOx has a reflectivity of about 3% and may be widely used does not remedy the aforementioned deficiencies of the applied reference combination.

Accordingly, reconsideration and withdrawal of this rejection of claims 5, 6, 9, 10, 20 and 21 are respectfully requested.

Reply to Response to Arguments

The Office Action states that “there is no black matrix between the upper substrate (60) and the pixel electrode (14) in the Fig. 2 . . .” Applicants respond by pointing out that Fig. 2 shows only part of the LCD. Figs. 4-6 disclose just the opposite, i.e., where the black mask 62 is directly above part of pixel electrode 14, and note that Morita is directed to “improve the aperture ratio of pixel” (col. 2, lines 6-7) and does this, in part, by providing an improved “black mask 62 [is] patterned in stripes on the opposing substrate. The black mask shields the gate lines 43, auxiliary lines 44 and this film transistors 3.” Thus, a black mask that is located

between the substrate and the pixel electrode is an essential part of Morita's invention, contrary to the quoted statement in the Office Action.

Applicants agree that Morita discloses placing a low-reflectance layer 10x on its highly reflective signal lines 10, but the Office Action fails to provide objective factual evidential support of proper motivation to modify Morita to provide this feature in Morita, as suggested, in lieu of Morita's improver black mask, for reasons stated above.

The admission by the Office Action that Hiraishi does not disclose providing a low reflectivity film on source, gate and drain electrodes of its switching transistors is telling. It is an indication that the secondary reference relied on to provide motivation to modify Morita to do the opposite and provide such a feature in Morita simply teaches away from doing what is suggested. Moreover, as pointed out above, the "same principle and same function" arguments may apply to the doctrine of equivalence for patent infringement analysis, but the issue involved here is proper motivation to modify primary reference that does not have this feature in view of a secondary reference that also does not have this feature, and this analysis simply does not fit.

Furthermore, one of ordinary skill in the art would have no incentive to modify Morita in view of Hiraishi, as suggested, because Morita's transistor electrodes are all shielded by the Morita's "improved" black mask and do not need the features provided by the low reflectance material. Additionally, the Office

Action fails to address the additional masking and etching steps that may be needed to provide such a suggested feature, steps that may well give a disincentive to provide such a feature.

Lastly, the argument regarding Inoue which states that because transistor electrode are electrical conductive films and different electrical conductive films are covered with low reflectivity films to improve reflective LCD performance, it would be obvious to provide low reflectivity coatings on the transistor electrodes overlooks the fact that none of the applied references, including Inoue provides low reflectivity coatings on transistor electrodes and overlooks the fact that Morita, the base reference, covers transistor electrodes with a black mask, thereby removing any need to modify Morita as suggested.

Conclusion

All of the stated grounds of rejection and objection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

Moreover, because the outstanding Office Action fails to address a number of Applicants' previously presented arguments in the Amendment filed on March 14,

Application No.: 09/550,282
Art Unit: 2871

Attorney Docket No. 0630-1524P
Reply to May 18, 2005 Office Action
Page 27

2005, Applicants are entitled to a supplemental Office Action or a New Office Action to address those issues.

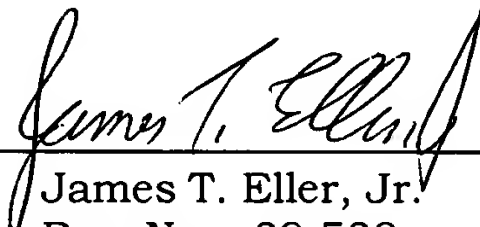
If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Robert J. Webster, Registration No. 46,472, at (703) 205-8000, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: 
James T. Eller, Jr.
Reg. No.: 39,538

JTE/RJW:pay/gf 

P.O. Box 747
Falls Church, VA 22040-0747
Telephone: (703) 205-8000